

Non-Zero and Open-Loop Current–Voltage Characteristics in Electronic Memory Devices

Febin Paul, Krishna Nama Manjunatha, and Shashi Paul*

This work focuses on the non-zero-crossing and open-loop current–voltage (I – V) characteristics of electronic memory devices that are studied and focused on primarily for non-volatile memory storage applications. Gold nanoparticles-based devices are fabricated to understand possible non-crossing zero and open-loop current–voltage behavior, where a non-zero current and open loop I – V characteristics are observed at zero voltage. While other studies have attributed this behavior as a “battery effect”, this study presents an alternate perspective for non-redox-based charge storage memory devices. The electrical measurements clearly demonstrate that the non-zero current and open-loop characteristics are due to the charge trapping of the gold nanoparticles. The charge accumulation within the nanoparticle is observed to create a non-zero potential within the device and thereby encouraging such behavior, even though the applied external voltage is zero. The longstanding mystery in deciphering if electrical measurements or the charge storage device contributes toward non-zero property is unfurled in this article. A possible charge storage model is proposed and further verified using liquid crystals-based two terminal devices. The presence of internal potential leads to an offset within the devices, a non-zero current and open-loop I – V even when the external applied voltage is zero.

the problems is the occurrence of the non-zero current at zero applied voltage and open-loop (I – V) behavior. Several works have attempted to explain the phenomena^[8–10] and some recent work has identified redox contributions to have the dominant effect for the observation of non-zero current at zero voltage,^[11] however, this still remain to be addressed in non-redox-based electronic memory devices.

The need for this work was observed a while ago when Saraf et al.,^[12] observed open circuit voltage in an epitaxial Fe doped SrTiO₃ (Fe:STO) deposited on Nb-doped SrTiO₃ (Nb:STO) device that was negatively biased. It was observed, however, that this open circuit voltage could be reset to zero by applying an external positive bias to the device. This result was however found to be significant in the light of a violation of the memristors,^[13] and memristive devices,^[14] which stated that since these devices were incapable of discharging energy, the I – V behavior must therefore cross the origin ($V = 0$ and


$I = 0$). The axiomatic relation between charge and flux in memristor was utilized by Biolek et al.^[8] to arrive at the conclusion that it must be zero-crossing.^[8] However, the only systematic study that addressed this issue until this date remains to be the study done by Valov et al.^[11] And even though the study explained the possible reason for non-zero I – V crossing systems, it confined the limits of the discussion to redox-based memory devices. The study presented the issue as being due to the migration of the ion, creating a chemical potential gradient that could result in a few hundreds of millivolt at zero volt condition.^[11] It was proposed based on this result that systems that do not obey zero-crossing can still be classified as memristor, as long as the equivalent circuit is substituted by an equivalent battery component to simulate the non-zero crossing behavior. And the non-zero-crossing was thus referred to as the “nano-battery effect”.^[10]

Paul et al. observed similar results in 2005, where the operation of the memory device was proposed to be due to the building-up of internal field.^[16] The model assumed the behavior to be due the formation of electric dipoles within the device that caused the current to be non-zero, even if the applied voltage was zero. This was further confirmed when nanocomposite devices were fabricated with C₆₀ molecules and insulating poly(4-vinylphenol) (PVP) showed a relative shift in the Raman analysis before and

1. Introduction

The past few years have seen an exponential rise in the study of electronic memory devices by the adoption of novel materials as information storage element and novel device structures. There are a number of mechanism by which information is stored and charge storage is one of them. Different charge storage behaviors are published every year, each differing in the device structure,^[1–5] active switching materials,^[6,7] etc. However, the field itself has been plagued by several problems. One of

F. Paul, K. Nama Manjunatha, S. Paul
Emerging Technologies Research Centre
De Montfort University
The Gateway, Leicester LE18BH, UK
E-mail: spaul@dmu.ac.uk

 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/aelm.202300324>

© 2023 The Authors. Advanced Electronic Materials published by Wiley-VCH GmbH. This is an open access article under the terms of the Creative Commons Attribution License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

DOI: 10.1002/aelm.202300324

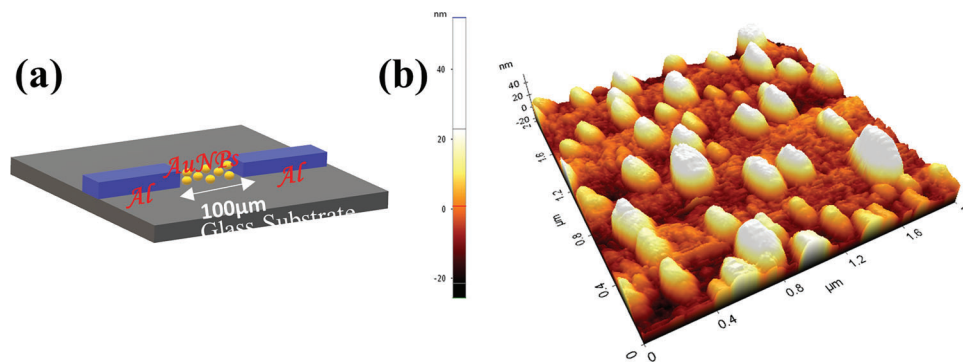


Figure 1. a) Shows the illustration of the gap cell structure that was used to test the devices. b) Shows the morphology of the gold nanoparticles using AFM. The nanoparticles clustered between the electrodes and it is not a single file of nanoparticles between the electrodes.

after a bias was applied to the device. The hysteresis observed in the device was therefore attributed to the charge storage by C_{60} molecule.^[16,17]

This is the underlying motivation for this work. Can a generalized approach, such as “nano-battery effect” be able to address the non-zero crossing in every system (for example, charge storage system or ferroelectric system)? Would a better understanding assist in a better accommodation of the device charge storage behavior? Some dedicated works have been presented to address the non-zero crossing systems^[9,15] a deeper analysis of the matter is felt. And for the first time, this work focuses on this issue using systems with multiple underlying mechanisms to address the non-zero crossing and open-loop I - V behavior.

In this article, results from gold nanoparticles suspended between the aluminum gap cells electrodes (test devices structures) have been analyzed to unfurl the mystery behind non-zero behavior observed in the I - V characteristics.^[24] The non-zero current at zero voltage is explained using the internal field model and the experimental results have been compared with theoretical results to verify and understand the anomalies in the charge storage in the devices and/or adopted measurement procedures. This result has been examined for the first time in the perspective of charge storage occurring in the inorganic nanoparticles and importantly non-redox-based memory devices. Furthermore, standard commercial liquid crystal device is experimentally characterized to explain the possible mechanisms and obtain greater insight toward non-zero-crossing behavior that is similar in most charge storage memory devices. It is worth mentioning that device architecture and the active material used in the liquid crystal devices (displays) are similar to two-terminal charge storage electronic memory devices. Their working principle is based on the field effect (explicitly – twisted nematic field effect) within the simplistic device structure thus eliminating the influencing factors that may arise from complex devices structures.

2. Experimental Section

The glass (corning-2875) substrates were sequentially cleaned using decon-90, acetone, and iso-propyl alcohol (IPA) followed by De-Ionized water (18 M Ω) in an ultrasonic bath for 30 min in each solvent. Glass substrates were then dried using stream of nitrogen gas and baked in an oven at 100 °C for 15 min. Aluminum electrodes were evaporated on the glass substrates using shadow

mask with 100 μ m gap between the electrodes. This device structure would be termed as gap-cell device in this manuscript. Edwards AUTO-306 thermal evaporator with a base pressure of $\approx 9 \times 10^{-7}$ mbar was used in this work. Aluminum wire (99.999%) purchased from Kurt J. Lesker was evaporated at a rate of 5 nm s⁻¹ to obtain 100 nm Al thin film electrodes. The gold nanoparticles (Au-NPs) suspension stabilized in citrate buffer purchased from Sigma–Aldrich (product code- 741957, diameter –10 nm) were sonicated in ultrasonic bath to reduce agglomeration and obtain uniform distribution in the solvent. Au-NPs were drop casted at 100 μ m gap between the electrodes (**Figure 1a**) by dispensing 500 nL solvent and then allowed to naturally dry in a laminar flow bench.

I - V measurements were performed with computer controlled HP4140B pico-ammeter. Electrical measurements of the aforementioned devices were performed at room temperature in EM-shielded probe station with 0.05 V step size with a time interval 0.01 s between consecutive voltage steps. Morphology of the AuNPs was studied from PISA XE-100 (Park Systems) scanning probe microscope in non-contact tapping mode.

The liquid crystal results were obtained from a commercially available liquid crystal display (LCD), Lumex LCD-S401C52TR.

3. Results and Discussion

3.1. Gold Nanoparticle Nanocomposite Devices

I - V measurements of the gold nanoparticles gap cell device are shown in **Figure 2a**. The magnitude of the current being within a few nanoamperes shows that the metallic part of nanoparticles is not in contact with each other. It must be noted that the nanoparticles are kept apart from each other due to their ligands attached to them.

Figure 2a shows the I - V behavior when the voltage sweep ± 1 V started at 0 V (bias sweep is applied as 0 to 1 to 0 to -1 to 0 V) and the arrows are shown in **Figure 2a** denoting the sequence of measurement. The non-zero I - V behavior can be clearly seen in **Figure 2a**, when a pristine device is measured beginning from 0 V; an open loop curve is observed at the end of the measurement revealing a non-zero current at zero applied voltage. However, when the device is measured starting from a non-zero applied voltage value (0.5, 1, 1.5, and 2 V) and sweeping back in a loop (**Figure 3a**), it can be observed that the system never takes the path

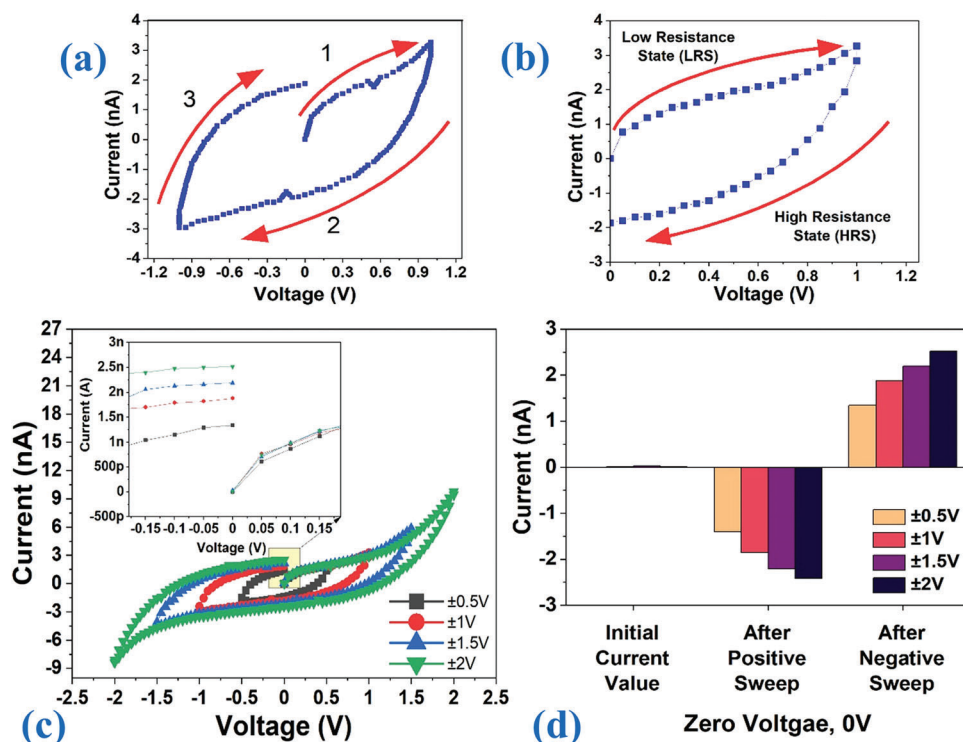


Figure 2. a) Current–Voltage behavior shown when the measurement begins at 0 V pristine state; the arrows denote the sequence of measurement. The resultant I – V curve is an open loop. b) The I – V behavior shows a transition from HRS to LRS. c) I – V measurement for multiple voltage sweep window reveal a nested behavior. The hysteresis in each case seems to be a function of the voltage sweep window. The inset shows the current value at zero volt. d) The graph shows the value of current at zero volt for three cases: before the measurement, after the positive sweep, and after the negative sweep. In each case the zero-voltage–current value seem to depend on the sweep window.

that it would normally take when the initial measurement was taken beginning from zero volt, leading to a closed loop behavior.

Similar results were observed in 2005 by Paul et al., where the operation of the memory device was proposed to be due to the building-up of internal field.^[16] Even though the non-zero crossing wasn't discussed explicitly, the model assumed trapping of

charges by any species (nanoparticles, as discussed in this work) led to the accumulation of charge, which in turn enhanced the internal electric potential of the device. This was further confirmed when nanocomposite devices were fabricated with C_{60} molecules and insulating poly(4-vinylphenol) (PVP) showed a relative shift in the Raman analysis before and after a bias was applied to the

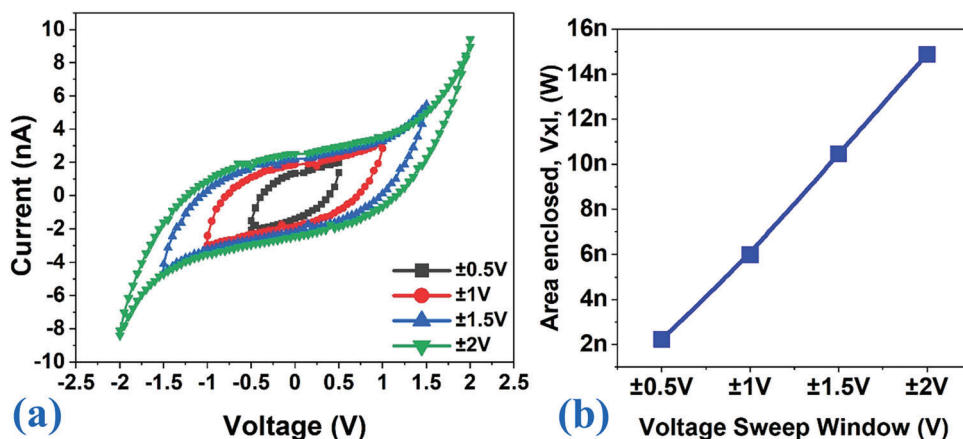


Figure 3. a) The plot shows a nested view of the current–voltage (I – V) behavior obtained from gold nanoparticles drop-cast gap cell devices; the measurement was initiated from a non-zero applied voltage (0.5, 1, 1.5, and 2 V), and the resultant I – V curve shows a closed loop characteristics showing that the device does not return to the current value at the pristine state. b) Shows a linear relationship between the voltage sweep window and the area enclosed by the I – V curve, showing that the hysteresis of the curve increases with increase in the maximum applied voltage.

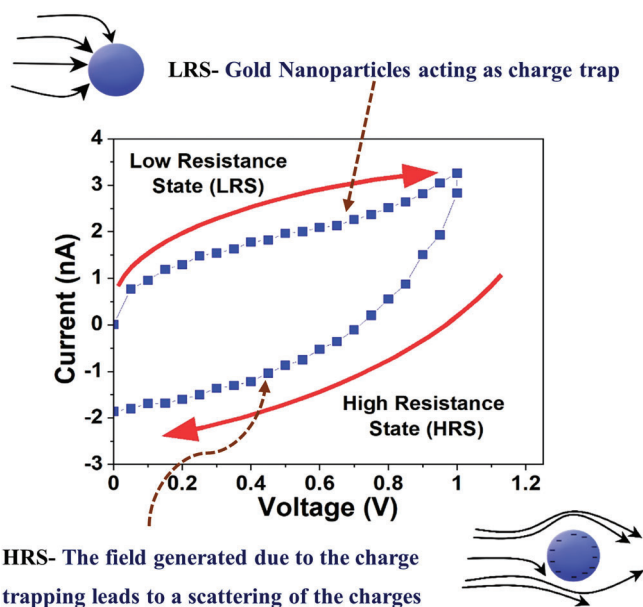


Figure 4. The figure shows the relationship between the LRS and HRS to the underlying charge transport. In the LRS, no opposition to the charge flow is experienced and the nanoparticles act as charge storage. However, in the reverse voltage sweep, the charge centers in nanoparticles begin to exert opposition to the flow of charge leading to a decrease in the flow of current and a HRS.

device. The hysteresis observed in the device was therefore attributed to the charge storage by C_{60} molecule.^[16,17] The non-zero-crossing of the curve in Figure 2a attests to a similar “electric potential build-up”, and the hysteresis shown in the Figure 2b confirms the presence of internal field. Figure 2b shows the device conduction behavior observed in the gold nanoparticle gap cell device; from the I - V behavior it can be evidently seen that the current measured during forward sweep is higher than the reverse sweep current thereby reflecting a transition from a low

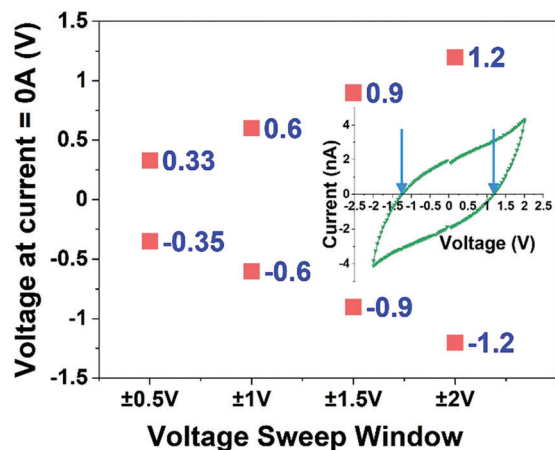


Figure 5. Plot shows the relationship of the voltage sweep range on the “remnant” voltage, at which current is zero. The higher the voltage sweep range, the higher the magnitude of voltage at which current is zero. The inset shows arrows indicating to the values of voltage that has been plotted.

resistance state (LRS) to a high resistance state (HRS). To put the significance of this result in context, a device that experiences conduction switching due to filamentary formation would experience a switching from HRS to LRS.^[18] Similar results can be seen in electrochemical metallization (ECM)-based systems as well.^[19] It can therefore be argued that the tendency of the device to switch from LRS to HRS arises from a different mechanism that has been addressed in the published literature.^[20] The observation, here, corresponds with the investigation performed by Prime and Paul using an Electrostatic Force Microscopy (EFM) analysis on isolated gold nanoparticles by applying 10 V to the device and using the Atomic Force Microscopy (AFM) tip to scan over the nanoparticle to check for electric field build-up.^[21] It was observed that the nanoparticle was able to capture the charges and trap it for a longer duration. The operation mechanism of this device was revisited by Paul in 2007,^[22] where a unique model was proposed to be responsible for the device behavior. It was proposed that the conduction switching and consequently the hysteresis in the I - V characteristics was due to the building up of electric field within the device. The necessity of such an explanation was due to the uniqueness of the I - V behavior of the device. Unlike other devices, the conduction switching observed in this study wasn't sharp, but smoothly incremental,^[22] including the absence of negative differential resistance (NDR) region.^[23] Referred to as the O -curve,^[23] similar device conduction switching behaviors were reported by several other works, like for example, Alotaibi et al. observed similar behavior in using selenium nanoparticles,^[24] Saranti et al.,^[25] in Silicon nanowires (SiNWs) and other researchers.^[24,25] In each of these devices, the charges injected within the active material are trapped by the defect (for example, in nanowires) and this charge trapping leads to the scattering of the charges being injected into the device due to accumulation of charges in the nanoparticles and/or nanowires. It was also reported that the area enclosed by the I - V curve was proportional the external voltage sweep window that has been exerted on the device.^[26]

The charge storage that corresponds with the hysteresis, was reported to be a function of the applied voltage. As the applied voltage increased, charges could be tunneled into the nanoparticles, as observed by Prime and Paul.^[21] This was confirmed by measurements on the isolated AuNPs between the Al gap electrodes. Figure 2c shows the nested I - V behavior obtained from the device when the voltage sweep window is gradually increased. As the voltage sweep window is increased, the current at zero voltage value proportionally increases. The non-zero value of current at zero voltage when a device has been measured for a full cycle ($0\text{ V to }+V_{\text{max}}$, $+V_{\text{max}}$ to 0 V , $0\text{ V to }-V_{\text{max}}$, and $-V_{\text{max}}$ to 0 V) is shown in Figure 2d. Figure 2d shows the value of current at zero voltage for different conditions. The first condition shows the current values at 0 V before the voltage sweep begins, the current values are significantly lower than the values obtained after the completion of measurement at 0 V . But, the magnitude and polarity of the zero-voltage-current depends on the voltage sweep window and the polarity of voltage that is applied to the device. The bar graph shows that after a positive and the negative voltage sweep, the current value at zero-voltage value is negative and positive, respectively. Moreover, as the value of maximum applied voltage increases, the value of the zero-volt current increases proportionally. Apart from evidencing a charge-based mechanism, this

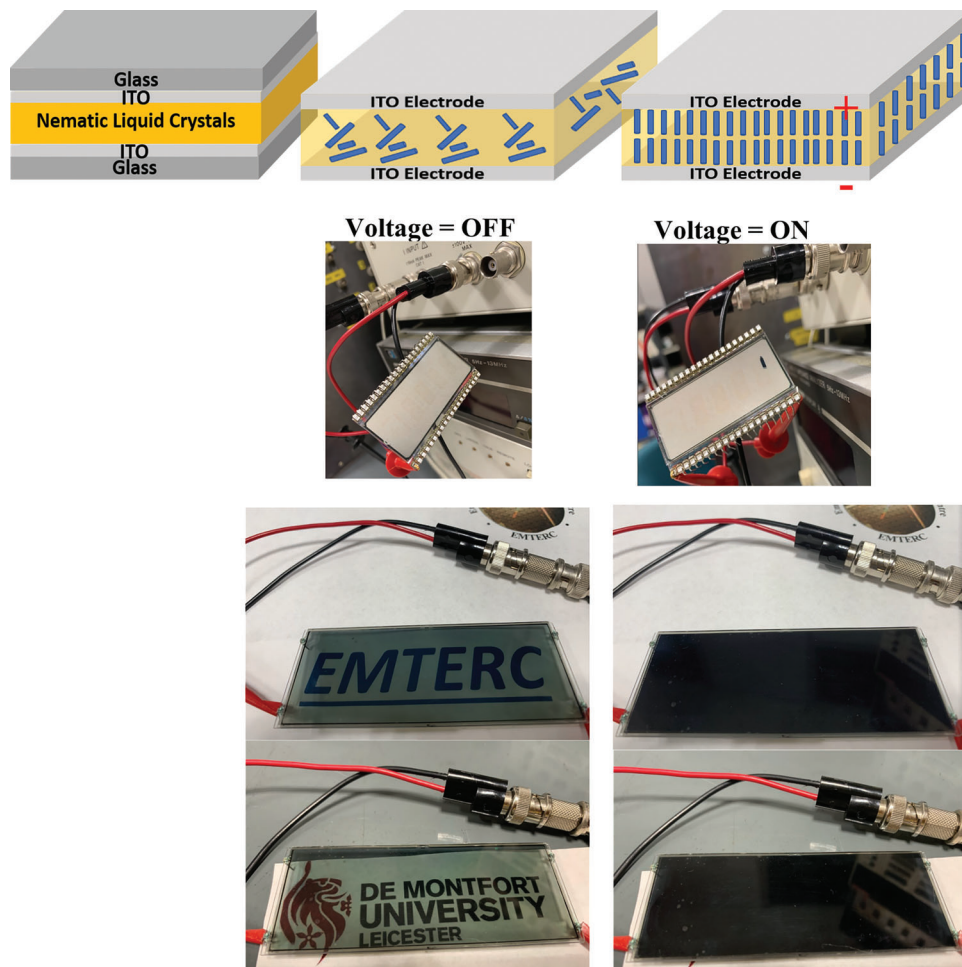


Figure 6. Image shows the illustration of TN-LCDs using 3D diagrams (top). The images show the LCD display functioning in the absence (transparent) and presence (black) of an external applied potential.

property can be used to achieve multi-conduction states for futuristic memory applications, such as neuromorphic memory.^[27,28]

It was observed that if the measurement was permitted to start at a non-zero voltage (Figure 3a), then the curve trajectory is quite distinct from that observed in Figure 2c, wherein the curve obtained in this case are close-looped. In a close loop I - V behavior, end current value is always same as the initial current measured at the beginning of sweep, whereas in Figure 2c, the final state of the system is quite different from the pristine state. However, in both cases, the device doesn't follow the zero-crossing and the hysteresis increases with the increasing sweep window; further represented as area enclosed by the curve (Figure 3b). Area is determined by integrating the I - V curve.

However, in the case of gold nanoparticles device measured in this work, the potential build-up is approximately estimated by the magnitude of applied potential at which the current becomes zero. The applied field in this case, is akin the coercive field, beyond which the polarization of the device switches.^[29] It could be proposed that due to the voltage sweep, charges populate the nanoparticles; the process followed by a gradual build-up of internal electric field within the system. This bias begins to compete with the applied bias in a manner that when it is equal and

opposite, resulting in the standstill flow of electrons. The zero current can be understood as being the result of zero potential difference across the device due to the internal bias; even though the applied external bias is non-zero. The difference in current flow in the presence of the charged nanoparticles give rise to a charge flow opposition and charge scattering, which can be interpreted as the HRS (refer Figure 4). Paul^[22] proposed a similar model for electron donor-acceptor system, where a charge dipole can cause enhanced scattering of charges after a voltage bias has been applied to the device.

The "coercive" voltages at which the current becomes zero have been plotted together with the sweep window of the input voltages (see Figure 5). In each measurement, there are two values of approximately equal and opposite values of voltages at which current become zero. The voltages represent estimate of the "internal electric field build-up" that got cancelled by the applied external electric field. It can thus be seen that the "coercive field" increases with the increase in the applied sweep, indicating toward an increase in charge trapping as the maximum applied voltage is increased. Once the device is swept over the positive range of voltage, the current becomes zero at a positive voltage (see Figure 5). From the internal electric field "build-up" perspective, this would

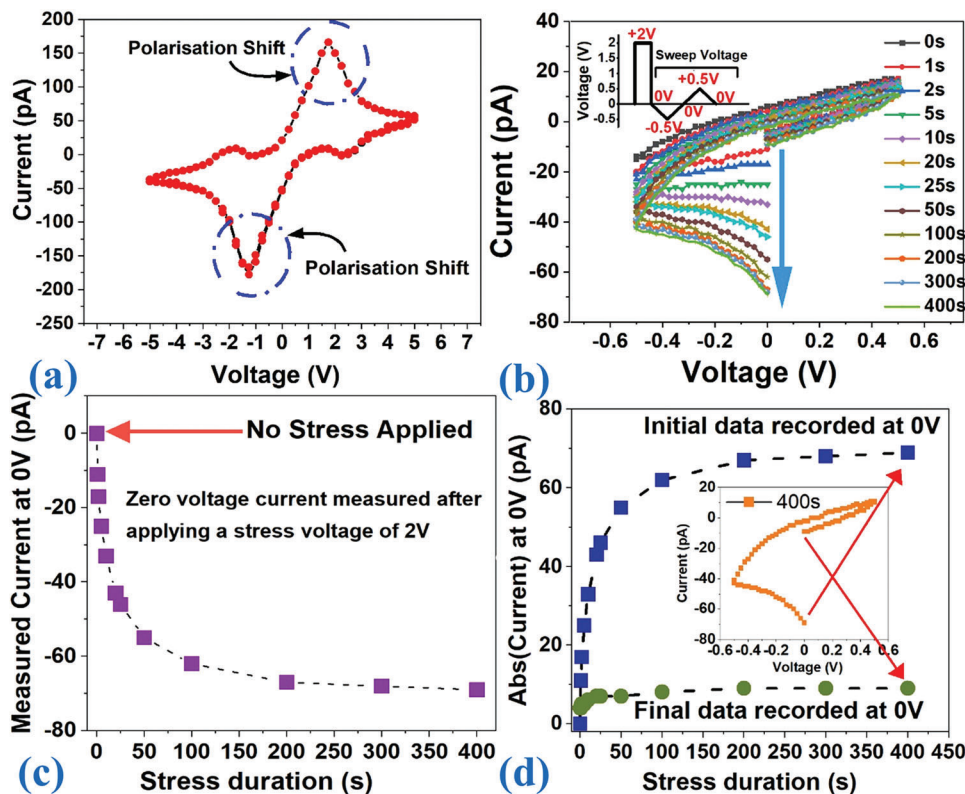


Figure 7. a) The I - V plot for the LCD has been shown between ± 5 V. The peak observed at each polarity represents the sudden switching of the dipoles in the direction of the applied electric field. The applied pulse magnitude of 2 V was chosen for the reason that, at 2 V most of the dipoles would have aligned themselves in the direction of the applied electric field. But as the duration of the pulse is increased, more and more domains that has a higher time constant respond by aligning themselves in the direction of the applied electric field. This is evidenced by the increased magnitude of the current at 0 V (as shown in Figure 7b). b) The I - V after a stress voltage of 2 V has been applied. The stressing time has been varied and the resultant I - V has been plotted between ± 0.5 V. c) The current value at 0 V was plotted against the stress time. d) The current value at 0 V has been measured in the beginning and end of the measurement. There are some smaller peaks in (a); this may result from the partial alignment of the electric dipoles of the LCD with the applied electric field.

clearly mean that the internal bias that compensated the external bias would be equal and opposite; the internal bias after applying a positive value of voltage across the device is measured negative. This is further supported from the Figure 2d at zero volts, the internal bias creates a DC bias. A negative bias in this case and therefore a negative value of current is observed at 0 V if an external positive voltage bias was applied across the device. Figure 2d provides clear evidence; when the measurement began at 0 V, the current observed was not high as it was by the end of the sweep measurement stopping at 0 V. subsequently, this explanation can equally describe the device behavior in the negative values of external bias.

However, in this case, instead of electrons populating the nanoparticles, the negative applied bias forces the trapped electron out from the nanoparticles; thereby leading to a positive current at 0 V and a zero-current occurrence in negative applied voltage.

3.2. Twisted Nematic Liquid-Crystal Devices

Apart from gold nanoparticles device, some measurements were undertaken on twisted nematic liquid-crystal devices to provide

further insight and strengthen the arguments proposed and discussed earlier. Liquid Crystals (LCs) are a well-understood system, and lie between the solid crystals that can achieve long-order arranged lattice and isotropic liquid with no regular arrangement.^[30] LCs can achieve orientational order when an external electric field is applied due to the polarization of the molecules (Figure 6).^[30]

The measurement in the following sections were conducted using a commercial LCD display (Lumex LCD-S401C52TR). The LCD display in this case was a twisted nematic (TN) type display, wherein the LCs can be vertically aligned when an external field is applied. In the switched OFF condition, the LCs assume a horizontal alignment where they are able to twist the light polarization by 90° . This is because a TN-LCD is a parallel plate capacitor with nematic crystals as the non-conducting dielectric. The crystals possess multiple quasi-stable relative permittivity which is dependent on the applied external voltage.^[31]

The I - V measurements were conducted with the LCD to check the device conduction and has been plotted in Figure 7a. The shift in the crystal polarization is visible between 1.5 and 2 V when the measurement was undertaken for complete forward and reverse sweep from +5 to -5 V. The effect of the applied external bias

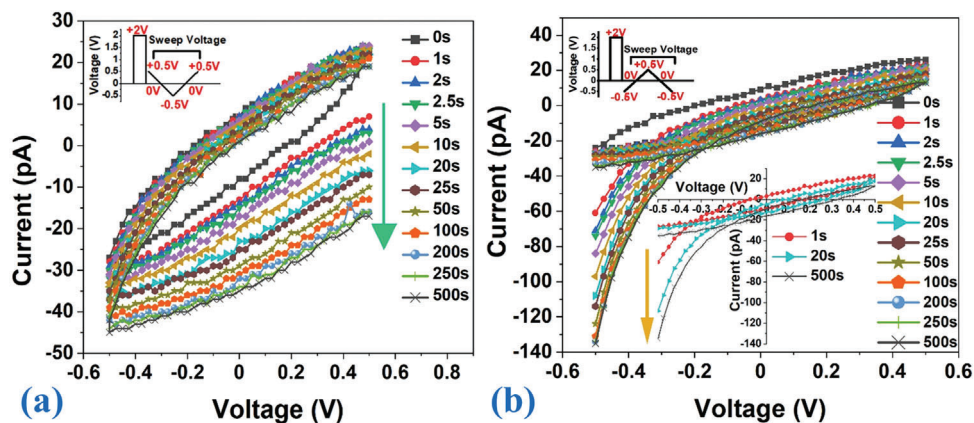


Figure 8. Effect on the I - V curve when the device is swept beginning from a) a positive bias (0.5 V) and beginning from b) a negative bias (-0.5 V). The inset in each graphs show the sequence of the measurement along with the applied magnitude.

was assessed in the LC devices by first applying a stress bias and the I - V sweep was conducted to assess the effect of the stress on the device conduction. Since the peak occurs at ≈ 2 V, any voltage pulse of this magnitude will cause a reorientation of the polarity within the LCD. Therefore, LC devices were stressed at 2 V for different durations. Immediately after this pulse, a voltage sweep was conducted, starting at 0 V and cycled back to 0 V. As the stress voltage is applied for longer durations, increasingly a greater number of crystals orient themselves in the direction of the electric field. This orientation of the crystals affects the magnitude of current that flows through the LCD during the I - V

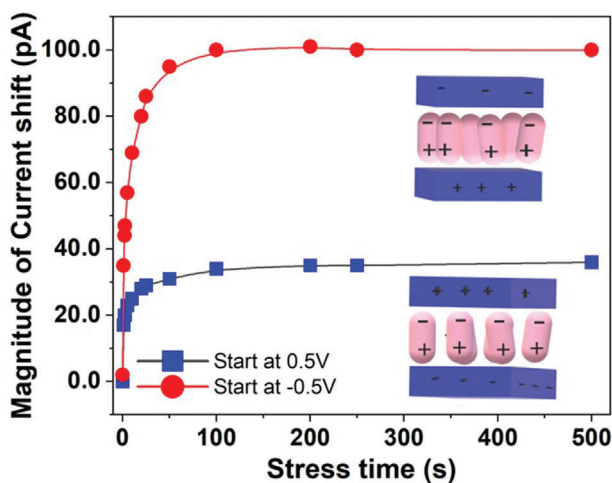


Figure 9. The plot shows the conduction shift due to the voltage stress. The square shaped data points show the current change when the voltage sweep is started with 0.5 V and the circle shaped data points show the current shift when voltage sweep begins with -0.5 V. It can be seen that when 0.5 V is applied, the internal field compensates the applied external field so that the current measured is relatively less. But, when the applied voltage polarity is reversed the internal field adds with the applied field and the resultant current is considerably higher. The change in the current is measured also when no stress is applied (0 s) which shows no current whether the sweep begins at 0.5 or -0.5 V. This shift in the current can thus be attributed toward the internal field generated due to the polarization of the liquid crystal.

sweep. This change was reflected in the I - V curves that followed the stress bias, wherein the greater the stress time, the greater was the value of current measured at 0 V (Figure 7b).

This shift in the internal potential build-up can be assessed by the change in the current at 0 V as was plotted separately against the stress time in Figure 7c. The plot shows an increase in the current with increase in the alignment of a greater number of crystals. The greater the stress time, crystals have greater amount of time to align in the direction of the applied field. The better the alignment, the better the charge accumulation due to the polarization of nematic crystal dipoles between the electrodes. However, it can be seen that as the stress time is increased, the measured current eventually reaches a saturation point where majority of the crystals are polarized. The current increase also attests to this change wherein the change in the electric conduction eventually reaches a saturation point. The change in the current in this case is similar to the all-organic devices that were characterized by Paul, wherein it was found that the change in the device conduction was not due to physio-electronic properties.^[16,17] The conduction switching was found to be due to an electronic transition at a molecular level, identical to the polarization shift that results due to the bond transition and electronic redistribution.

The effectiveness of the charge redistribution due to the polar alignment of dipoles within the LC was tested by comparing the current values at the beginning of the measurement and at the end of the measurement. As can be seen in Figure 7b, the mode of the measurement was to start at $V = 0$ and continue to $+0.5$ V, back to -0.5 V before cycling the voltage sweep back to 0 V. And while the shift in the current is evidently influenced by the stress bias, the effect of this stress is lost halfway between the measurements due to the scattering of the polar alignment due to the measurement itself. Due to this the final sweep of all the curves fall in the same region (i.e., measured current -6 ± 3 pA). Due to this the final value of current was compared with the initial value of current (both measured at 0 V) and plotted in (Figure 7d). It can therefore be seen that while the first record of current at zero volt is a function of the time for which the applied voltage is applied, the final current reading (which loops back at zero volt) is relatively similar for all the measurements; the voltage sweep and duration of the sweep itself interferes with the initial state of the system.

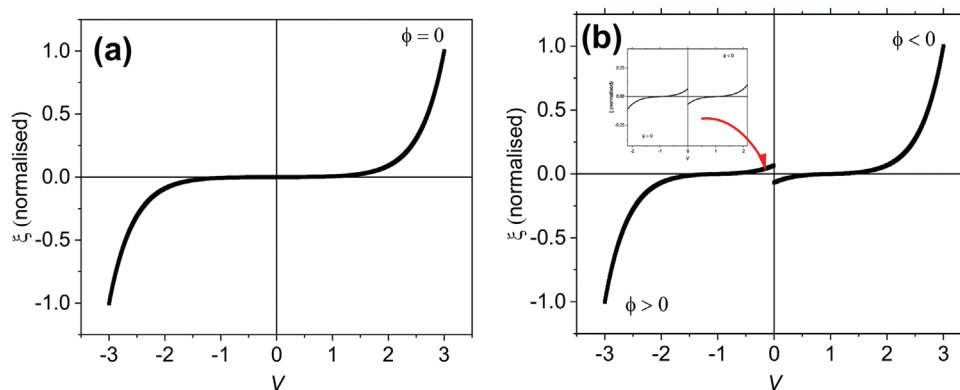


Figure 10. Current–Voltage behavior of a) a device without any internal electric field ($\phi = 0$) generated during the voltage scan b) a device have internal electric field created (ϕ is negative for all values of $V > 0$ and positive for all values of $V < 0$). It clearly shows an open loop behavior and a negative current for a value below a certain positive voltage value and a positive current for a value below a certain negative voltage value.

The LC device is similar to the gold nanoparticle device in regard to the discussion that in both the devices the application of an electric field leads to the accumulation of charges that themselves then compete with the external applied field. And even though the exact mechanism of how this happens is different in each of these cases, the final output is the same. In LC, the accumulation of charges is due to the crystal alignment and the polarization, but in the gold nanoparticles, the charge build-up is due to the trapping of the electrons by the nanoparticles during the sweep measurements.

The effect of the internal electric field competing with the external applied bias (or in other words external electric field) can be visualized by following a simple experiment. **Figure 8**, shows the device conduction when the voltage is swept in different sequence, even though the applied stress voltage is the same in both the scenarios. Since the stress voltage applied in both the sweep scenarios is 2 V, it can be safely assumed that the polarity of the crystal alignment will be same. However, in one case the device is swept beginning with the positive bias (left), while the other device is swept starting from the negative bias (right). If the internal field hypothesis is correct then the internal field due to the polarization of the LC would compete in one of the cases and add up with the applied bias in the other case, which would in turn reflect in the magnitude of current that would be measured.

The difference in the current at 0 V, at the beginning of the measurement and the end of the measurement, was recorded and plotted against the stress time. Under normal circumstances with no voltage stress being applied, the current value is expected to be as similar, compared to the beginning and end of the measurement, i.e., the change in current at the beginning and at the end of the measurement will be zero. This is found to be true in both the cases, whether the voltage sweep was started at 0.5 or -0.5 V (refer **Figure 9**). However, when the stress bias is applied to align the nematic crystals within the device, the current value of the device depended on the polarity of the initial polarity and magnitude of the external applied voltage and the polarity of the internal alignment of nematic crystals.

As seen in **Figure 9**, the magnitude of current increase due to the stress bias is different depending on the polarity of the applied

signal. It must be noted that the reference point (0 s stress) shows the change to be minimal, but when the voltage sweep begins with 0.5 V, the internal field compensates the applied external field due to the opposite polarity, hence the current is relatively less. But, the current when the device is swept beginning -0.5 V is greatly higher due to the adding up of the internal field and the applied field. This demonstrates how the internal field of the device affect the conduction behavior.

For a better understanding of this, we can represent the observed current–voltage behavior in the following mathematical form:

$$\xi(V) = aV + b e^{(c V \mp \phi)} \quad (1)$$

where $\xi(V)$ is the current, V is the applied voltage, and a , b , and c are arbitrary constants. Establishing values of arbitrary constants is possible through the use of boundary conditions and bistable system under study. Please note that Equation (1) is a mathematical model, we do not assume any particular electrical conduction mechanism in our devices, but we used it to explain the observed electrical behavior. ϕ is really important parameter, it determines if there is an internal electric field ($\phi \neq 0$) or not ($\phi = 0$). The origin of ϕ can be based on the points discussed earlier in this article. **Figure 10** is obtained based using Equation (1) for mimicking whether the internal electric field is present ($\phi \neq 0$) or not ($\phi = 0$) in the device. The results obtained are very similar to the real devices tested in this work; negative current at certain positive bias voltage and positive current at certain negative bias voltage and open loop are all resembling the devices tested in this work. Therefore, ϕ gives a control over the memory devices, e.g., we can think of conceiving ϕ which is invariable over a period of time and therefore, retaining the memory state. Or we can choose ϕ to diminish after a certain period of time (e.g., seconds to hours or days to months, etc) and will result in self-destructing memory devices especially when someone is carrying sensitive information one place to other. We can also conceive ϕ in such a way that it varies with some external electric field stress value applied to devices and, therefore, resulting in the plastic nature of the device subjected to the test. So, we can build on that concept to create neuromorphic memory.

4. Conclusion

This work has focused on the value of the non-zero current at zero voltage. Gold nanoparticle-based gap cell measurements show that the non-zero current at zero voltage depended on the voltage sweep window applied to the device. This non-zero crossing behavior was explained based on the internal field model that the non-zero value of current at zero voltage was due to the build-up of potential within the nanoparticles. The charge-trapping behavior of the gold nanoparticle was the cause of the non-zero current. This explanation was further substantiated by measurements taken from liquid-crystal display devices. It was found that similar non-zero current were observed when a bias voltage was applied to align the liquid crystal. The longer duration of the bias stress voltage applied; it was observed that the magnitude of the current at zero voltage increased, demonstrating that the current values reflected the alignment of the liquid crystals and therefore was proportional to the net polarization of the crystals. The non-zero current was observed due to the non-zero internal potential that was developed when subjected to external bias voltage. The magnitude of the current saturated after ≈ 100 s of bias stress voltage, which further demonstrated that the liquid crystal polarization was saturated at this point and hence the current magnitude also saturated. This paper has presented an alternate perspective to the non-zero current for non-redox-based system, where the “nano-battery effect” may not be applicable. A thorough understanding of ϕ will help us to design memory devices which may lead to immortal memory or self-destructive memory devices or neuromorphic memory devices.

Acknowledgements

S.P. would like to thank EPSRC (grant #EP/E047785/1) for supporting this work.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

liquid crystal memory, memristors, non-volatile memory, non-zero crossing, non-zero I - V characteristics, open-loop electrical behaviors, two-terminal memory

Received: May 16, 2023

Revised: July 3, 2023

Published online:

- [1] M. Di Ventra, Y. V. Pershin, *Mater. Today* **2011**, *14*, 584.
- [2] A. Chen, *Solid-State Electron.* **2016**, *125*, 25.
- [3] T. C. Chang, K. C. Chang, T. M. Tsai, T. J. Chu, S. M. Sze, *Mater. Today* **2016**, *19*, 254.
- [4] R. J. Tseng, C. Tsai, L. Ma, J. Ouyang, C. S. Ozkan, Y. Yang, *Nat. Nanotechnol.* **2006**, *1*, 72.
- [5] J. Ouyang, C. W. Chu, C. R. Szmanda, L. Ma, Y. Yang, *Nat. Mater.* **2004**, *3*, 918.
- [6] T. Zhang, X. T. Zhang, L. L. Wu, H. Gao, N. Zhang, Z. T. Zhang, A. C. Balazs, B. Yang, C. T. Zhang, F. W. Liu, G. H. Li, H. Y. Xu, J. T. Zhang, J. Aizenberg, M. Y. Zhang, *Nanoscale Adv.* **2019**, *1*, 2718.
- [7] Y. Li, C. Zhang, Z. Shi, C. Ma, J. Wang, Q. Zhang, *Sci. China Mater.* **2021**, *65*, 2110.
- [8] D. Birolek, Z. Birolek, V. Birolekova, *Electron. Lett.* **2011**, *47*, 1385.
- [9] B. Sun, M. Xiao, G. Zhou, Z. Ren, Y. N. Zhou, Y. A. Wu, *Mater. Today Adv.* **2020**, *6*, 100056.
- [10] L. Qingjiang, A. Khat, I. Salaoru, C. Papavassiliou, X. Hui, T. Prodromakis, *Sci. Rep.* **2014**, *4*, 4522.
- [11] I. Valov, E. Linn, S. Tappertzshofen, S. Schmelzer, J. van den Hurk, F. Lentz, R. Waser, *Nat. Commun.* **2013**, *4*, 1771.
- [12] S. Saraf, M. Markovich, T. Vincent, R. Rechter, A. Rothschild, *Appl. Phys. Lett.* **2013**, *102*, 022902.
- [13] L. Chua, *IEEE Trans. Circuit Theory* **1971**, *18*, 507.
- [14] L. O. Chua, S. M. Kang, *Proc. IEEE* **1976**, *64*, 209.
- [15] B. Sun, Y. Chen, M. Xiao, G. Zhou, S. Ranjan, W. Hou, X. Zhu, Y. Zhao, S. A. T. Redfern, Y. N. Zhou, *Nano Lett.* **2019**, *19*, 6461.
- [16] S. Paul, A. Kanwal, M. Chhowalla, *Nanotechnology* **2006**, *17*, 145.
- [17] A. Kanwal, S. Paul, M. Chhowalla, *Mater. Res. Soc. Symp. Proc.* **2005**, *830*, 349.
- [18] L. Ma, J. Liu, S. Pyo, Y. Yang, *Appl. Phys. Lett.* **2002**, *80*, 362.
- [19] J. Ouyang, *Emerging Resistive Switching Memories*, Springer, Berlin, Germany **2016**.
- [20] F. Paul, S. Paul, *Small* **2022**, *18*, 2106442.
- [21] D. Prime, S. Paul, *Appl. Phys. Lett.* **2010**, *96*, 043120.
- [22] S. Paul, *IEEE Trans. Nanotechnol.* **2007**, *6*, 191.
- [23] D. Prime, S. Paul, *Philos. Trans. R. Soc., A* **2009**, *367*, 4141.
- [24] S. Alotaibi, K. N. Manjunatha, S. Paul, *Appl. Surf. Sci.* **2017**, *424*, 330.
- [25] K. Saranti, S. Paul, *ACS Appl. Electron. Mater.* **2019**, *1*, 2018.
- [26] Z. A. Halafi, S. Paul, I. Salaoru, S. Alotaibi, *MRS Adv.* **2017**, *357*, 195.
- [27] V. S. Reddy, S. Karak, A. Dhar, *Appl. Phys. Lett.* **2009**, *94*, 88.
- [28] M. T. Ghoneim, M. A. Zidan, K. N. Salama, M. M. Hussain, *Microelectron. J.* **2014**, *45*, 1392.
- [29] Q. D. Ling, D. J. Liaw, C. Zhu, D. S. H. Chan, E. T. Kang, K. G. Neoh, *Prog. Polym. Sci.* **2008**, *33*, 917.
- [30] J. Prakash, S. Khan, S. Chauhan, A. M. Biradar, *J. Mol. Liq.* **2020**, *297*, 112052.
- [31] G. W. Gray, S. M. Kelly, *J. Mater. Chem.* **1999**, *9*, 2037.